REMARKS/ARGUMENTS

Claims 1-30 are pending in the present application.

This Amendment is in response to the Office Action mailed August 24, 2004. In the Office Action, the Examiner rejected claims 1-7, 8, 9-17, 18, 19-27, 28, 29 and 30 under 35 U.S.C. §103(a). Claims 1, 11, and 21 have been amended. Reconsideration in light of the remarks made herein is respectfully requested.

Rejection Under 35 U.S.C. § 103

In the Office Action, the Examiner rejected claims 1-7, 9-17, 9-29, 29, and 30 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent Application Publication US2002/0052999 issued to Jahnke et al. ("Jahnke") in view of U.S. Patent No. 6,260,093 issued to Gehman et al. ("Gehman"), claims 1-7, 11-17, 21-27 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,619,661 issued to Crews et al. ("Crews") in view of Gehman, and claims 8, 18, and 28 under 35 U.S.C. §103(a) as being unpatentable over Jahnke in view of Gehman, as applied to claims 1-7, 9-17, 19-27, 29, and 30 above, and further in view of U.S. Patent No. 5,941,968 issued to Mergard et al. ("Mergard"). Applicant respectfully traverses the rejection and contends that the Examiner has not met the burden of establishing a prima facie case of obviousness.

Applicant reiterates the arguments presented in the previous response. Specifically, Applicant contends that Jahnke and Gehman, or Crews and Gehman, taken alone or in combination, at least fail to disclose, suggest or render obvious (1) a processor interface circuit interfacing to a second processor having accessibility to the first and second buses, and (2) an arbitration logic circuit to arbitrate access requests from the first and second processors.

1. In response to Applicant's arguments, the Examiner states that the Examiner is taking both arbiters/decoders 314 and 316 of Jahnke to be Applicant's arbitration logic circuit. The Examiner further states that since Applicant's claims do not recite any language that precludes this interpretation, Examiner believes that the current application of the Jahnke reference to the claim is reasonable and correct (Office Action, page 8, item 6, page 9). Applicant respectfully disagrees. The claim language clearly recites: "an arbitration logic circuit...to arbitrate access requests from the first and second processors." This language clearly precludes the use of two

different and separate arbiters to arbitrate requests from two processors, one for each. The article "an" indicates a singular noun, not a plural noun.

Claims should be interpreted consistently with the specification, which provides content for the proper construction of the claims because it explains the nature of the patentee's invention. See Renishaw P.L.C. v. Marposs Societa Per Azioni, 158 F.3d 1243 (Fed. Cir. 1998). Here, the claims recite "an arbitration logic circuit...to arbitrate access requests from the first and second processors." This claim language is further supported by the specification. See, for example, Figure 2B, elements 150, 110, and 160; Figure 3; Page 7, paragraph [0028]. Both the claim language and the specification indicate that there is only a single arbitration logic circuit, not two separate and different arbiters as taught or suggested by Jahnke.

2. The Examiner further states that Gehman was used to teach a second processor, not the processor interface and Jahnke was used to teach an interface circuit to a second master. However, as argued in the previous response, since Gehman does not teach or suggest a processor interface circuit, it cannot be combined with Jahnke. Furthermore, there is not a reasonable chance of success in combining the teachings when both references teach away from the claimed invention as argued previously.

3. The Examiner further states that "since there is no language in the claims which precludes the interpretation of both the primary and secondary arbiters of Crews as reading on the claimed arbitration logic circuit, it is the Examiner's position that this interpretation is reasonable and correct" (Office Action, page 9, last paragraph). Applicant respectfully disagrees. As discussed above, the claim language clearly recites an arbitration logic circuit to arbitrate access requests from the first and second processors, it precludes the use of two separate arbiters arbitrating requests from two processors separately.

4. The Examiner further states that Mergard was used to teach the advantage of having the second master of Jahnke be DMAC. However, the claim language recites that the second processor is a DMAC where the second processor has accessibility to the first and second buses. In contrast, Mergard teaches that the DMAC, the CPU, and the graphic controller share access to a unified system memory through a data bus, not accessible to first and second buses. Jahnke

does not disclose the second processor having accessibility to the first and second buses. Therefore, the combination of Jahnke and Mergard does not read on the claim language.

Therefore, Applicant believes that independent claims 1, 11, 21 and their respective dependent claims are distinguishable over the cited prior art references. Accordingly, Applicant respectfully requests the rejection(s) under 35 U.S.C. §103(a) be withdrawn.

Conclusion

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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